Claim 1 recites that the wiring board has a wiring board thickness. The warp preventing board is joined to the outer surface of the semiconductor chip and is composed of the same material as that of the wiring board. Claim 1 further recites that the warp preventing board has a warp preventing board thickness that is substantially equal to the wiring board thickness.

It is respectfully submitted that the rejection is improper because the applied art fails to teach each element of claim 1. Specifically, the applied art fails to teach a wiring board having a wiring board thickness and a warp preventing board having a warp preventing board thickness that is substantially equal to the wiring board thickness. Thus, claim 1 is allowable over the applied art.

Claim 2 depends from claim 1 and includes all of the features of claim 1. Thus, claim 2 is allowable at least for the reason claim 1 is allowable as well as for the features it recites.

Withdrawal of the rejection is respectfully requested.

Claim 3 is rejected under 35 U.S.C. 103(a) as unpatentable over Shirai et al. in view of Ball (U.S. Patent No. 6,165,815). The rejection is respectfully traversed.

Ball discloses, in Fig. 8 of his patent, a die assembly 800 that has a pair of substrates 606 and 808 which sandwich the chip-on-chip structure formed by a pair of dies 602 and 604 adhere to each other by a layer of an adhesive 618.

Claim 3 depends from claim 1 and includes all of the features of claim 1. Claim 3 is therefore allowable at least for the reason claim 1 is allowable as well as for the features it recites. Specifically, claim 3 recites that the warp preventing board is another wiring board and another semiconductor chip is electrically connected to the warp preventing board being joined to a surface, facing away from the semiconductor chip, of the warp preventing board. In other words, The Ball patent fails to disclose that a circuit board is joined to an inactive surface of a semiconductor chip. For least this additional reason, claim 3 is allowable over the applied art.

Withdrawal of the rejections is respectfully requested.

Claim 4 is rejected under 35 U.S.C. 103(a) as unpatentable over Shirai et al. in

view of Lee (U.S. Patent No. 6,303,997). The rejection is respectfully traversed.

Lee discloses, in Fig. 1 of his patent, a stacked, laminated semiconductor package unit that has a plurality of individual packages 100' stacked on top of each other. Each of the semiconductor package 100' has a printed circuit board 2', a semiconductor chip 1' bonded to the top surface of the printed circuit board 2', and solder balls 4' provided in a peripheral area on the lower surface of the printed circuit board 2'.

Claim 4 depends from claim 1 and includes all of the features of claim 1. Thus, claim 4 is allowable at least for the reason claim 1 is allowable as well as for the features it recites. Specifically, claim 4 recites a wiring material for electrically connecting the wiring board and the warp preventing board is interposed therebetween. In other words, Lee discloses a stacked structure of a plurality of semiconductor packages. However, there is a gap between the inactive surface of the semiconductor chip 1' and a printed circuit board 2', so that the printed circuit board never has a function for preventing warp of the semiconductor package 100'. Thus, claim 4 is allowable over the applied art for this additional reason.

Withdrawal of the rejection is respectively requested.

Furthermore, none of the applied art addresses problems solved by the present invention, the warping of the package as the environmental temperature changes. Therefore, none of the applied art teaches the measures adopted in the present invention. That is, according to the present invention, a semiconductor chip is sandwiched by a wiring board and a warp preventing board whose thickness is substantially equal to that of the wiring board. This feature is not disclosed or suggested in any of the cited art.

Additionally, the features of newly-added claim 5 are not taught or suggested in the applied art.

In view of the foregoing, reconsideration of the application and allowance of the pending claims are respectfully requested. Should the Examiner believe anything further is desirable in order to place the application in even better condition for

allowance, the Examiner is invited to contact Applicants' representative at the telephone number listed below.

Please charge any fee deficiency or credit any over payment to Deposit Account No.18-0013 that is necessary to consider an appropriate response timely filed.

Respectfully submitted,

Date: April 4, 2002

By _____
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Enclosure(s): Marked-Up Version of Amended Claim

DC086573

MARKED-UP VERSION OF AMENDED CLAIMS

1. (Amended) A semiconductor device comprising:

a semiconductor chip;

a wiring board joined to one surface of the semiconductor chip and electrically connected to the semiconductor chip, the wiring board having a wiring board thickness; and

a warp preventing board joined to the other surface of the semiconductor chip and composed of the same material as that of the wiring board, the warp preventing board having a warp preventing board thickness substantially equal to the wiring board thickness.